WHAT IS CLAIMED IS:

1. A fuse circuit for a semiconductor integrated circuit, comprising:

a plurality of fuses; and

a plurality of transmission circuits for transferring signals in response to a status of the fuses.

2. The fuse circuit of claim 1, wherein the plurality of fuses have an identical fusing status.

3. The fuse circuit of claim 1, wherein each of the fuses includes two ends in which one end is connected to power supply voltage.

4. The fuse circuit of claim 3, wherein the transmission circuits correspond to the fuses, each of the transmission circuits comprising:

a transmission gate having an input terminal, an output terminal, and a primary control terminal connected to the other end of a corresponding fuse, and a secondary control terminal; and

an inverter having an input terminal connected to the other end of the corresponding fuse and the primary control terminal, and an output terminal connected to the secondary control terminal.

5. The fuse circuit of claim 4, wherein the transmission gate includes:

a first conductive transistor having a first electrode connected to the input terminal, a control electrode connected to the other end of the corresponding fuse, and a second electrode connected to the output terminal; and

a second conductive transistor having a second electrode connected to the input terminal, a control electrode connected to the output terminal of the inverter, and a first electrode connected to the output terminal.

6. The fuse circuit of claim 4, wherein power supply voltage is applied to the input terminal.

7. The fuse circuit of claim 5, wherein each of the transmission circuits further comprises a resistor where one end is connected to the control electrode of the first conductive transistor and the input terminal of the inverter, and the other end is connected to the power supply voltage.

8. A fuse circuit storing information related to a semiconductor integrated circuit, comprising;

a plurality of fuses each of which has two ends in which one end is connected to power supply voltage, the fuses storing predetermined information relevant to the semiconductor integrated circuit; and

a plurality of transmission circuits, each connected to one of a respective other ends of the fuses for transferring an input signal to an output terminal in response to the predetermined information established by the fuses,

wherein the transmission circuits are connected in series.

9. The fuse circuit of claim 8, wherein the fuses store one-bit of the predetermined information relevant to the semiconductor integrated circuit.

10. The fuse circuit of claim 8, wherein each of the transmission circuits comprises:

a transmission gate having an input terminal, an output terminal, a primary control terminal connected to the other end of a corresponding fuse, and a secondary control terminal; and

an inverter having an input terminal connected to the other end of the corresponding fuse and the primary control terminal, and an output terminal connected to the secondary control terminal.

11. The fuse circuit of claim 10, wherein the transmission gate includes:

a NMOS transistor having a drain connected to the input terminal, a gate connected to the other end of the corresponding fuse, and a source connected to the output terminal; and

a PMOS transistor having a source connected to the input terminal, a

gate connected to the output terminal of the inverter, and a drain connected to the output terminal.

12. The fuse circuit of claim 11, wherein the transmission circuit further comprises a resistor where one end is connected to the control electrode of the NMOS transistor and the input terminal of the inverter, and the other end is connected to power supply voltage.